IN THE CLAIMS:

Please amend Claim 21 as follows:

21. (Currently Amended) A circuit for amplifying an input signal close to a ground voltage or a negative supply voltage, the circuit comprising:

a differential difference amplifier having first and second differential input pairs, the first differential input pair coupled across a voltage to be amplified;

a first load device coupled between first and second inputs for the second differential input pair;

a second load device coupled in a feedback loop between an output for the differential difference amplifier and the second input for the second differential input pair; and

a voltage offset device coupled between an input for the first differential input pair and an input for the second differential input pair.

Please add new Claims 22-42 as follows:

PN 2 22. (New) The circuit as set forth in Claim 1 21 wherein said differential difference amplifier comprises:

a first non-inverting input terminal of said first differential input pair wherein said first non-inverting input terminal is capable of being coupled to said input signal;

a first inverting input terminal of said first differential input pair wherein said first inverting input terminal is capable of being coupled to said negative supply voltage;

a second inverting input terminal of said second differential input pair wherein said second inverting input terminal is capable of being coupled to said second load device coupled to an output of said differential difference amplifier;

a second non-inverting input terminal of said second differential input pair wherein said second non-inverting input terminal is capable of being coupled to said offset voltage device;

a first differential transistor pair comprising a first transistor having a gate coupled to said first non-inverting input and a second transistor having a gate coupled to said first inverting input;

a second differential transistor pair comprising a third transistor having a gate coupled to said second non-inverting input and a fourth transistor having a gate coupled to said second inverting input;

a first cascode transistor pair comprising a fifth transistor having a gate coupled to said first non-inverting input and a source coupled to a drain of said first transistor and a sixth transistor having a gate coupled to said first inverting input and a source coupled to a drain of said second transistor; and

a second cascode transistor pair comprising a seventh transistor having a gate coupled to said second non-inverting input and a source coupled to a drain of said third transistor and an eighth transistor having a gate coupled to said second inverting input and a source coupled to a drain of said fourth transistor.

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3 ~~23~~. (New) The circuit as set forth in Claim 2 ~~22~~ wherein said a source of said first transistor and a source of said second transistor are coupled to the output of a first bias current generating source.

4 ~~24~~. (New) The circuit as set forth in Claim 3 ~~23~~ wherein a bulk connection of said first transistor and a bulk connection of said second transistor are coupled to an offset voltage of said offset voltage device.

5 ~~25.~~ 4 (New) The circuit as set forth in Claim ~~24~~ wherein a bulk connection of said fifth transistor and a bulk connection of said sixth transistor are coupled to said sources of said first and second transistors.

6 ~~26.~~ 5 (New) The circuit as set forth in Claim ~~25~~ wherein a source of said third transistor and a source of said fourth transistor are coupled to the output of a second bias current generating source.

PN

7 ~~27.~~ 6 (New) The circuit as set forth in Claim ~~26~~ wherein a bulk connection of said third transistor and a bulk connection of said fourth transistor are coupled to a positive supply voltage.

8 ~~28.~~ 7 (New) The circuit as set forth in Claim ~~27~~ wherein a bulk connection of said seventh transistor and a bulk connection of said eighth transistor are coupled to said sources of said third and fourth transistors.

9 ~~29.~~ 8 (New) The circuit as set forth in Claim ~~28~~ wherein a drain current of said fifth transistor and a drain current of said seventh transistor are combined to produce a first composite current.

10 ~~30.~~ 9 (New) The circuit as set forth in Claim ~~29~~ wherein a drain current of said sixth transistor and a drain current of said eighth transistor are combined to produce a second composite current.

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11 ~~31.~~ 10 (New) The circuit as set forth in Claim ~~30~~ further comprising a current difference detection circuit in said differential difference amplifier wherein said current difference detection circuit is capable of detecting a current difference in said second and first composite currents and generating an output voltage that is proportional to said current difference.

PN 12

~~32.~~ (New) A battery monitoring apparatus comprising:

a sensor coupled to a battery such that a charge current flows through said sensor when said battery is charging and a discharge current flows through said sensor when said battery is discharging;

an offset voltage generation circuit capable of generating an offset voltage;

a differential difference amplifier for amplifying a voltage sense signal on said sense resistor and adding said offset voltage to the amplified voltage sense signal, said differential difference amplifier having first and second differential input pairs, the first differential input pair coupled across said voltage sense signal to be amplified;

a first load device coupled between first and second inputs for the second differential input pair;

a second load device coupled in a feedback loop between an output for the differential difference amplifier and the second input for the second differential input pair; and

wherein said offset voltage generation circuit is coupled between an input for the first differential input pair and an input for the second differential input pair.

13 ~~33~~. (New) The battery monitoring apparatus as set forth in Claim 12 ~~32~~ wherein said PN differential difference amplifier comprises:

a first non-inverting input terminal of said first differential input pair wherein said first non-inverting input terminal is capable of being coupled to said input signal;

a first inverting input terminal of said first differential input pair wherein said first inverting input terminal is capable of being coupled to said negative supply voltage;

a second inverting input terminal of said second differential input pair wherein said second inverting input terminal is capable of being coupled to said second load device coupled to an output of said differential difference amplifier;

a second non-inverting input terminal of said second differential input pair wherein said second non-inverting input terminal is capable of being coupled to said offset voltage generation circuit;

a first differential transistor pair comprising a first transistor having a gate coupled to said first non-inverting input and a second transistor having a gate coupled to said first inverting input;

a second differential transistor pair comprising a third transistor having a gate coupled to said second non-inverting input and a fourth transistor having a gate coupled to said second inverting input;

a first cascode transistor pair comprising a fifth transistor having a gate coupled to said first non-inverting input and a source coupled to a drain of said first transistor and a sixth transistor

having a gate coupled to said first inverting input and a source coupled to a drain of said second transistor; and

a second cascode transistor pair comprising a seventh transistor having a gate coupled to said second non-inverting input and a source coupled to a drain of said third transistor and an eighth transistor having a gate coupled to said second inverting input and a source coupled to a drain of said fourth transistor.

14 ~~34.~~ (New) The battery monitoring apparatus as set forth in Claim ~~33~~ 13 wherein said a source of said first transistor and a source of said second transistor are coupled to the output of a first bias current generating source.

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15 ~~35.~~ (New) The battery monitoring apparatus as set forth in Claim ~~34~~ 14 wherein a bulk connection of said first transistor and a bulk connection of said second transistor are coupled to an offset voltage of said offset voltage generation circuit.

16 ~~36.~~ (New) The battery monitoring apparatus as set forth in Claim ~~35~~ 15 wherein a bulk connection of said fifth transistor and a bulk connection of said sixth transistor are coupled to said sources of said first and second transistors.

17 ~~37.~~ (New) The battery monitoring apparatus as set forth in Claim 16 ~~36~~ wherein a source of said third transistor and a source of said fourth transistor are coupled to the output of a second bias current generating source.

18 ~~38.~~ (New) The battery monitoring apparatus as set forth in Claim 17 ~~37~~ wherein a bulk connection of said third transistor and a bulk connection of said fourth transistor are coupled to a positive supply voltage.

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19 ~~39.~~ (New) The battery monitoring apparatus as set forth in Claim 18 ~~38~~ wherein a bulk connection of said seventh transistor and a bulk connection of said eighth transistor are coupled to said sources of said third and fourth transistors.

20 ~~40.~~ (New) The battery monitoring apparatus as set forth in Claim 19 ~~39~~ wherein a drain current of said fifth transistor and a drain current of said seventh transistor are combined to produce a first composite current.

21 ~~41.~~ (New) The battery monitoring apparatus as set forth in Claim 20 ~~40~~ wherein a drain current of said sixth transistor and a drain current of said eighth transistor are combined to produce a second composite current.

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22 ~~42.~~ (New) The battery monitoring apparatus as set forth in Claim 21 ~~41~~ further comprising a current difference detection circuit in said differential difference amplifier wherein said current difference detection circuit is capable of detecting a current difference in said second and first composite currents and generating an output voltage that is proportional to said current difference.